Article

A TCAD Study on κ-Graded Stacked Gate Oxides on Tri-gate FinFETs

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**Abstract:** Since its invention in the 1960s, one of the most significant evolutions of metal-oxidesemiconductor field effect transistors (MOSFETs) would be the three dimensionalized version that makes the semiconducting channel vertically wrapped by conformal gate electrodes, also recognized as FinFET. During the past decades, the width of fin (Wfin) and the neighboring gate-oxide width (tox) in FinFETs has shrunk from about 150 nm to a few nanometers. However, both widths seem to have been levelling off in recent years, owing to the limitation of lithography precision. Here, we show that by adapting Penn model and Maxwell-Garnet theory for dielectric constant (κ) calculation method for nanolaminate structures, 2- and 3-level κ-graded stacked combinations of gate dielectrics with SiO2, SiN, HfO2, La2O3, TiO2 on a 14nm FinFET are simulated and compared for performance against same structure with single layer dielectrics. Based on this, FinFETs with κ-graded gate oxides, achieved ION/IOFF ratios around 1012 and IOFF current reaching down to 10-16 A and gate leakage current reaching down to 10-13 A. Our findings push the individual dielectric laminates to the sub 1 nm limit and may shed light on the next generation nanoelectronics for higher integration and lower power consumption.

**Keywords:** κ-graded stacked gate oxides; stacked high-κ gate-oxide dielectrics, Technology Computer-Aided-Design (TCAD) Simulation; Functionally Graded Material (FGM); Fin-Field Effect Transistors (FinFET); threshold voltage (**V**TH), on-state current (**I**ON), off-state current (**I**OFF), drain-induced barrier lowering (**DIBL**) and subthreshold slope (**SS**), **I**ON/IOFF ratio and gate metal-to-silicon leakage current (**IG**).

1. Introduction

Silicon oxide has been used as a gate dielectric material for over 40 years, but as transistor dimensions shrink, alternatives with higher dielectric constants are needed to reduce leakage currents. High-k dielectrics like HfO2, ZrO2, Al2O3, and others have been investigated for their thermal stability and compatibility with Si. FinFET technology, with 3D double-gate and triple-gate transistors, has further advanced, leading to smaller, more efficient transistors with reduced power consumption [1], [2], [3], [4], [5], [6], [7], [8], [9].

The continuous downscaling of MOS devices is essential for increasing transistor density and performance, leading to efficient chip functionality at higher speeds. However, this scaling poses challenges such as severe short channel effects (SCEs), increased fabrication costs, and difficulties in device processing [10-15]. Multi-gate MOS device structures like FinFETs, which use multiple gate electrodes and an ultrathin body, have been developed to address these challenges, showing excellent device performance at scaled parameters. An important aspect of FinFET structures is threshold voltage tuning and its sensitivity to different device parameters. Studies have shown that threshold voltage is insensitive to doping variation in nanoscale MOSFET structures, leading to a preference for engineering the work function of gate materials rather than increasing body doping. The use of metal gates has become attractive due to their chemical stability with high-k gate dielectrics and the ability to maintain higher threshold voltages while acquiring high gate stack stability [16], [17], [18], [19], [20], [21].

Research of graded dielectrics on thin film transistors first appeared in 1994 by Kuo when SiNx laminates with different dielectric deposition conditions were tried and compared with single SiNx as gate dielectric [22]. In a patent by Gartner et.al in 2000, a 3-layer graded dielectric film is formed on an upper surface of the semiconductor substrate. A second dielectric film is then formed on the first dielectric film. A third dielectric film is then formed on surface of the second dielectric film. The first, second, and third dielectric films are then annealed along with the semiconductor substrate by immersing into an inert ambient maintained at a temperature in the range of approximately 600-1100 C. The second thickness and the second dielectric constant were kept greater than the first thickness and the first dielectric constant and the third thickness and the third dielectric constant also were greater than the second thickness and the second dielectric constant respectively. An equivalent oxide thickness of the first, second, and third dielectric films are each in the range of 5-15 angstroms. The first dielectric film comprises a silicon dioxide film having a thickness of approximately 5 angstroms. The second dielectric film comprises silicon nitride. Thickness of the second dielectric film is in the range of approximately 10-20 angstroms. The third dielectric constant is in the range of approximately 10-200, and the third thickness is in the range of approximately 25-250 angstroms. The third dielectric film is an oxide comprising oxygen and a dielectric impurity with one of the elements Be, Mg, Ca, Ti, Zr, or Ta [23]. This work is the main cornerstone and first sign of commercialization of the graded dielectric research upon thin film transistors. Subject has has been already mature as many patents filed and commercializations issued after then on FinFETs with graded dielectrics.

Stacked laminates of gate-oxides on FinFETs have been investigated in several research works. Lorenzo et.al proposed a gate engineered oxide stack silicon on insulator (SOI) FinFET device with a high-κ dielectric gate oxide stack structure, which improved the analog and RF performance of the device compared to standard single gate oxide structures [24]. Das et.al proposed a dual-material-gate dual-stacked-gate dielectrics gate-source overlap Germanium FinFET with low leakage current, high on drain current, and high ratio of on current to off current [25]. Bousari et.al demonstrated in simulation that dual and triple heterogate dielectric structures act well on triple-gate FinFETs [26]. Similar work and simulations were also addressed in papers [27], [28]. Gangwani et.al analyzed the temperature performance of a stacked oxide top-bottom gated junctionless FinFET, which showed enhanced output performance and reduced short channel effects compared to conventional junctionless FinFET [29]. The influence of fin geometry on corner effects in multifin dual and tri-gate SOI-FinFETs , benchmarking of FinFET [30], nanosheet, and nanowire FET architectures for future technology nodes, the analog performance analysis of stacked oxide top-bottom gated junctionless FinFET [29] and a detailed study of single-material gate, double-material gate, and triple-material gate FinFETs were carried out. In-depth analysis of typical types of FinFETs were presented in [20] with which we tried to match the terminology and abbreviations within this paper [31]. Among existing methods Maxwell-Garnet equation [32] for calculation of effective κ for 2-layer dielectrics. As we need 3-layer effective κ calculation we need to derive the two equations for 3-layer dielectrics.

In this paper we introduce functional gate dielectrics consisting of 2- or 3- layer known dielectrics working on FinFETs, which might be candidate for fabrication on top of Si-channeled FinFETs.

Our research focused on conducting simulation-based studies of performance of FinFET technology, including geometrical modeling of inverse u-shaped dielectric devices and analytical modeling of kappa kalculations.

Modified Penn Model [33], [34] is used to calculate the dielectric constant of thin nanolaminate material forming each FGM laminate, using their bulk dielectric constant bandgap energy EG, high frequency dielectric constant and its Fermi wave vector *K*f. Maxwell-Garnet (MG) approximation [32] is selected to calculate the effective dielectric constant () for the 2-and 3-layered FGM dielectrics. Quantum tunneling model and Hot Electron / Hot Hole Injection (HEI-HHI) models [35] are used to model gate leakage current within SILVACO ATLAS/Deckbuild simulation tool and results were found to be consistent with experimental results within [36] with systematically varying thickness of mentioned dielectric layers to form a graded structured 3 nm-thickness FGM gate dielectrics. FinFET Buried Oxide (BOX) material was kept as Al2O3 through all simulations.

In this work, simulations were performed with single and double FGM dielectric materials for trigate FinFET structure. Our research focused on conducting a simulation-based study of FinFETs since their introduction in the year 2000 [19], performance of FinFET technology, including analytical modeling and simulation of FinFET devices [8], the influence of fin geometry on corner effects in multifin dual and tri-gate SOI-FinFETs [14], benchmarking of FinFET, nanosheet, and nanowire FET architectures for future technology nodes [30], the analog performance analysis of stacked oxide top-bottom gated junctionless FinFET [29] and a detailed study of single-material gate, double-material gate, and triple-material gate FinFETs were carried out [31]. In-depth analysis of typical types of FinFETs were presented in [20] with which we tried to match the terminology and abbreviations within that paper.

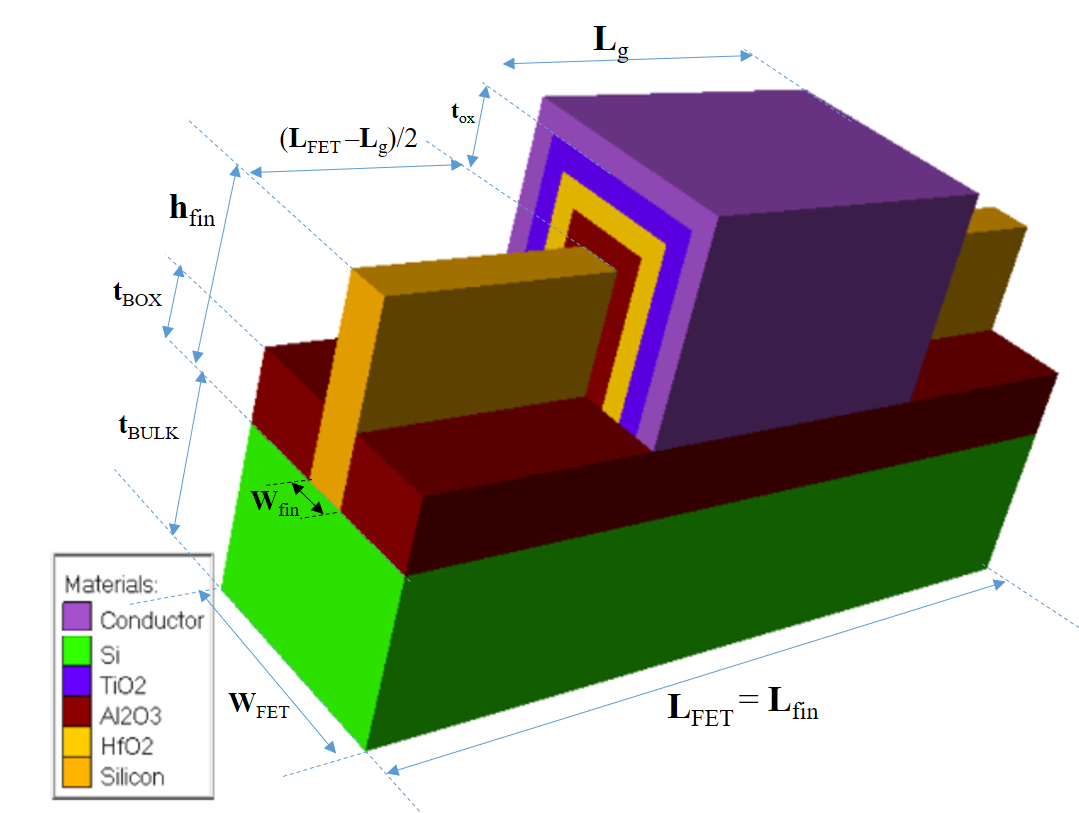
The binary system of Ta2O5 and Nb2O5 has been investigated as a dielectric material, and a Ta2O5/Nb2O5 bilayer with a high dielectric constant of 50 can be prepared by a 500°C fabrication process [1]. Additionally, glasses of the system TeO2/Nb2O5/ZnO have been studied, and the dielectric constant of the 85 and TeO2/10Nb2O5/5ZnO glass was found to be 66, which is higher than that of pure TeO2 glass and other binary systems [2].

Thus it becomes challenging to achieve simple binary oxide dielectric between the dielectric constant (κ) greater than 35 (of Nb2O5) and less than 95 (of TiO2). Here emerges the opportunity to generate materials with κ in the range of 35-95 through utilization of κ-grading in gate dielectrics. Studies show multi-material stacked gate-oxides continue to demonstrate their potential as semiconductor-to-gate insulators, yet in these studies the effective dielectric constant () calculation step and effect of κ-ordered stacking is vastly ignored. In this paper, taking these two factors into account, we present simulation results obtained using TCAD tools for a 3-D silicon on insulator (SOI) n-FinFET structure with various gate dielectrics with “κ-graded stacking” in FinFET geometries by utilizing of the dielectric stack. In conjunction with studies on stacked laminates of gate-oxides like SiO2, Al2O3 and HfO2, this study further explores role of ordered stacking of oxide laminates towards gate metal with increasing κ value, artificially forming a κ-graded functionally graded material (FGM).

2. Description of Device Structure

The 3D Technology Computer-Aided Design (TCAD) structure for FinFETs is shown in Fig. 1.

Using SILVACO ATLAS for device simulation, we start with SiO2, Al2O3, HfO2, La2O3 and TiO2 as single layer gate dielectrics of 3 nm thickness (tox) for a 14nm channel (fin) length (LFET), 2 nm channel width (WFET), 5 nm channel height (hfin) FinFET structure, then formed 13 different FGM materials with systematically varying thickness of mentioned dielectrics to form a graded structured 3 nm-thickness gate oxide dielectric. With thickness of 3 nm, BOX material (Figure 1) is kept as Al2O3 and never changed through simulations. Equal doping concentration of 5x1019 cm–3 is used source - drain channel region.



Buried Oxide (BOX) on Silicon

Gate

Channel

**Figure 1.** Proposed 3-material FGM gate oxide dielectric based **G**κ-FinFET

**Table 1.** Proposed **G**κ-FinFET properties.

|  |  |  |
| --- | --- | --- |
| Property | Value | Note / Abbreviation |
| Channel (Fin) Length | 14 nm | Lfin |
| Gate thickness | 10 nm | Tg |
| Channel (Fin) Width | 2 nm | Wfin |
| Gate Length | 14 nm | Lg |
| Fin Width | 2 nm | Wfin |
| Fin Height | 5 nm | Hfin |
| Channel Concentration | 5x1019 cm-3 | Nd |
| Gate work function | 5 eV | φw |
| FET Length | 34 nm | LFET |
| FET Width | 10 nm | WFET |
| Total Gate Oxide thickness | 3 nm | tox |
| BOX Thickness | 3 nm | tBOX |
| BOX material | Al2O3 | - |
| Bulk Si Thickness | 10 nm | tBULK |

Figure 2. depicts the cross-sectional view of the Gκ-FinFET implemented using stack approach. The design parameters considered for the device are depicted in Table 1. Both the device structures are of n-type FinFET, comprising of two gates, control gate and polarity gate which are isolated in nature. The control gates and the polarity gates are used for modulation of effective tunnelling barrier width. The Work function of 5 eV, is applied at the control gate thus converting n + layer under the control gate into intrinsic region and a work function of 5.93 eV is applied at the polarity gate, thus, converting n + layer under polarity gate into p+, which acts as the source region. Thus, n + −n + −n + region is converted into n + −i–p + region which works as n + −i–p + FinFET. The work function of 5.93 eV (Platinum) has been used at the source metal electrode in order to form the source region through concept of charge plasma, by inducing approximately 1019/cm3 of hole concentration on the silicon surface at the source side of device [26]. Similarly, the work function of 3.9 eV has been used at drain side, to form the drain region through charge plasma concept, by inducing electron concentration on silicon surface at drain side of device. All the parameters for FinFET same, with one main difference. In the case of the SO PG FinFET, (SiO2 + HfO2) stack is used, while in the case of PG FİNFET, only SiO2 stack is used. Both the positive and negative ITCs are applied at the silicon oxide interface.

The fixed charge density of ITCs is taken to be Nf = ±1.0 × 1012 /cm2 ) [25, 27, 28]. It should be noted that in the simulation, INTERFACE statement from [29] has been considered to analyze the density of interface fixed charges and their position available at interface of silicon and oxide layer.

INTERFACE statement has been implemented in Silvaco TCAD as follows:

INTERFACE QS=+1e12 x.min=0.020 x.max=0.040 y.min=- 0.0030 y.max=-0.0020.

Here QS represents the interface charge density, and it can be positive or negative, x represents the channel length position in μm and y represents channel width position in μm. Although the presence of interface traps is there at the interface of HfO2 and oxide layer in SO PG FinFET and will be absent in case of PG FinFET, but in present manuscript only the ITCs along the channel length at the silicon and oxide interface has been considered. The ITCs at the HfO2 and oxide interface has been neglected because, in case of TFETs mainly the impact of drain junction and the tunneling junction is there on the device behavior [23]. The spacer thickness, which is 5 nm between polarity gate and source and electrodes, finds how the gate field is closer to the tunneling path towards the source side. Thus, while finding the tunneling probability it becomes an important parameter. The impact of ITCs on the dc performance, analog/RF and linear distortion performance of both the PG FinFET and SO PG FinFET has been studied in this work. 2-D Silvaco Atlas device simulator has been used to conduct all the simulations. Shockley Read Hall and Auger models have been used in order to account for presence of highly doped impurity atoms in channel and minority recombination region. Nonlocal band-to-band tunneling (BTBT) model [30, 31], has been used, which analyses the rate of generation of carriers at each point. For implementing this model, region of quantum tunneling are defined at interface of source and channel and drain and channel interface, in order to account for ON state tunnelling of carriers, and ambipolar nature of FİNFET respectively. Use of bandgap narrowing model is done to account for high doping concentration in the channel region [20]. The quantum confinement model has also been applied, which is incorporated by using the Schrodinger Poisson model. The nonlocal BTBT model utilizes the isotropic tunneling effective mass of hole as well as the electron [32]. This model provides the solutions of Schrodinger’s equation, for the energies of the bound states in conduction bands and valence bands, as well as the solution of Poisson equation for electric potential. The Schrodinger’s equation solution also determines the quantum electron density calculations. Quantum electron density calculations have to be solved for wave function as well as magnitude of Eigen state energy at each cross section of the device. Fermi Dirac model has been used to calculate electron and hole concentrations, as well as wave function and Eigen energy [32]. These parameters have been utilized for calculating the potential using Poisson’s equation [32]. Schottky tunnelling model has also been used. The nonlocal trap-assisted tunneling (TAT) model has been incorporated in order to account for TAT, which is based on the Wentzel–Kramer–Brillouin (WKB) transmission coefficient with an exact tunneling barrier [33]. This model utilizes the material parameters that is tunneling mass of hole considered as 0.16 and tunneling mass of electron considered as 0.21 [34].

ekran görüntüsü, diyagram, metin, çizgi içeren bir resim

Açıklama otomatik olarak oluşturuldu

**Figure 2.** Proposed 3-material FGM gate oxide dielectric based FinFET

metin, ekran görüntüsü içeren bir resim

Açıklama otomatik olarak oluşturuldu

**Figure 1. (a)** Fabrication steps

**(b)**

Fabrication Process

Fabrication of the FinFET can be done using nonplanar technologies. The procedure of fabrication as shown in Fig. 1(c) is explained as follows:

Fabrication of channel can be done by Bosch processes or deep reactive ion etching [32]; (ii) Deposition of gate oxide can be done by using low pressure chemical vapor deposition (LPCVD) [32]; (iii) The patterning of window, which defines region of tunneling can be done using plasma etching [35]; (iv) Successively, deposition of HfO2 layer can be done by using Atomic Layer Deposition at 200° C, which can be followed by annealing in O2 ambient [36]. (v) Formation of source/drain contact can be done by growing it epitaxially over the substrate [31]; Successively, patterning of the polarity gates (PGs) can be done by using the process of e-beam lithography [32]; and (vii) Finally, the spacer formation and contact deposition can be done [32].

3. Methods

As we target to prove that FGM gate oxide dielectric structures behave and perform better than single material dielectric structure in FinFET design, our method will be 5 steps. We need to analyze, model and evaluate the nanoscaled dielectric structures decreasing thickness will reduce the bulk capacitance and dielectric constant of the dielectric. First in IIIa, Modified Penn Model [33], [34] is used to calculate the dielectric constant of thin nanolaminate material forming each FGM laminate, using their bulk dielectric constant bandgap energy EG, high frequency dielectric constant and its Fermi wave vector *K*f. In part IIIb thru IIIc, Maxwell-Garnet (MG) approximation [32] is selected to calculate the effective dielectric constant () for the 2-and 3-layered FGM dielectrics. In IIId and IIIe, FinFET model in Figure 1 is implemented via ATLAS language and Hot Electron / Hot Hole Injection (HEI-HHI) model [35] is used to model gate leakage current within SILVACO ATLAS/Deckbuild simulation tools are used to calculate with experimental results within [36], with systematically varying thickness of mentioned dielectric layers to form a graded structured 3 nm-thickness FGM gate dielectrics. Eighteen different FinFET model simulationsare performed in Silvaco Atlas Deckbuild, first five models include single material gate oxide dielectrics in Table 4A and subsequent thirteen models include FGM dielectrics as gate-oxide (in Table 4B). Thru IIIf and IIIg, key electrical performance parameters like threshold voltage (**V**TH), on-state current (**I**ON), off-state current (**I**OFF), drain-induced barrier lowering (**DIBL**) and subthreshold slope (**SS**), **I**ON/IOFF ratio and gate metal-to-silicon leakage current (**IGL**) are selected and evaluated for each simulation. We also design a customized figure of merit in order to justly evaluate each FinFET performance with respect to each other. Here we present details each step as below:

3.1. Thickness Dependence of Under Quantum Confinement Effects

Theoretical foundation for constructing a -graded FGM is given in US Patent 8110469 by Gealy et.al. [37] and we model our gate oxide for FinFET as below:

metin, diyagram, ekran görüntüsü, çizgi içeren bir resim

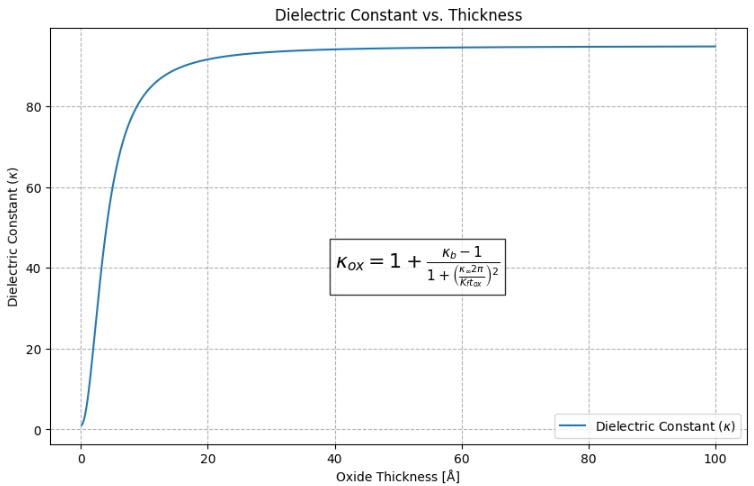
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**Figure 2.** Stepwise Grading Profile for an example FGM (FGM-H in Table 4B.) as gate oxide dielectric.

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Gate oxide dielectric constant has to be evaluated for according to the formula, Equation-1,

where is the bulk dielectric constant, is the high frequency dielectric constant, is Fermi wave vector, is the thickness of the nanoscaled dielectric material [33].

metin, diyagram, çizgi, öykü gelişim çizgisi; kumpas; grafiğini çıkarma içeren bir resim

Açıklama otomatik olarak oluşturuldu

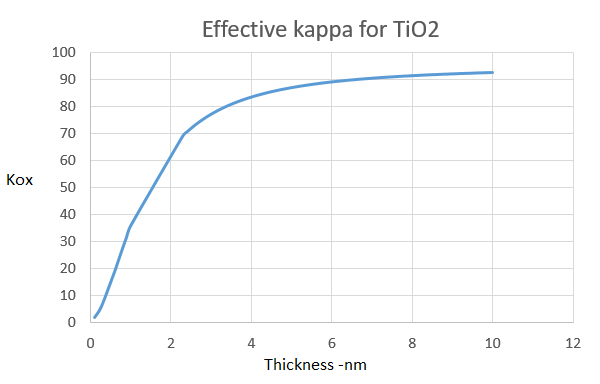
Iki grafiği tek grafikte birleştir ve yazılar daha okunur olsun.

**Figure 3.** Modified Penn Model for dielectric constant against thickness applied to TiO2 [33], [34].

For silicon (Si), it has been shown that for thicknesses greater than 10 Å (1 nm), bulk can be considered to be unchanged and equivalent to [34]. If is less than 10 Å then we need to consider generalized Penn model [38] for modelling dielectric constant as against thickness, under quantum confinement effects for nanolaminates for each FGM’s to be calculated correctly. As we herein try to model nanolaminates around 5-30 Å, we calculated of interlayer nanolaminate according to Equation-1. This can be numerically further fitted to the Equation-2 in [38] ;

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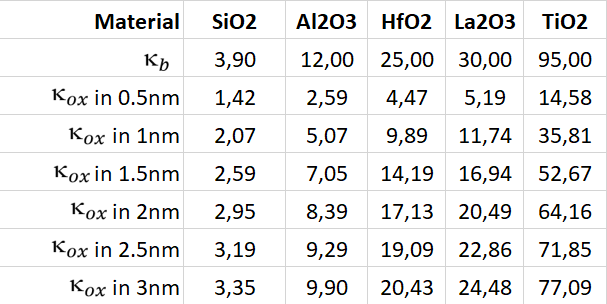
and when we calculate the resultant kappa of same material due to its nanolaminate thickness and observe the significant loss in dielectric effect when we observe Table-2. This numerical approximation is depicted in Figure 4, showing that in orders of few nanometers nanolaminate TiO2 thickness, kappa reduction is significant.



YENİDEN ÇİZİLECEK 2 eksen kullanılacak

**Figure 4.** A numerical approximation for Penn Model evaluated by Equation-2.

**Table 2.** Bulk dielectric constant and resultant oxide kappa with respect to nanolaminate thickness *tox* of dielectric materials calculated with Equation-2.

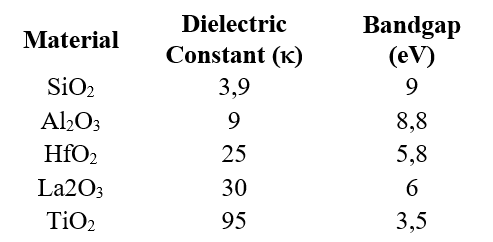


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3.2. Modelling Oxide Nanolaminates as FinFET Gate oxide Dielectrics

In order to isolate the gate metal and form a proper electric field to control the drain current, gate dielectrics are of great importance. Dielectric constants (κ) of some selected gate oxides vary from 3.9 to 95 and their respective bandgaps vary from 9 eV down to 3.5 eV in Table 3.

**Table 3.** Bandgap and dielectric constant for simple binary oxides used in this paper [22], [23.]



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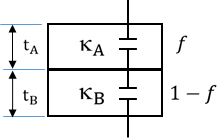
HfO2 thin films have wide band gap of ≈ 5.8 eV, high dielectric constant (κ ≈ 25) and suitable band offset values relative to Si substrate. In addition to their excellent thermodynamic and chemical stability, HfO2 has been strongest candidate material for replacing single layer SiO2 gate dielectrics. There exists no simple binary oxide dielectric between the κ greater than 35 (of Nb2O5) and less than 95 (of TiO2). Thus there starts the possibility and opportunity to generate materials with κ in the range of 35-95 through FGMs, that have the potential to show better performance properties than HfO2, especially when we utilize a method to calculate the equivalent dielectric constant of the stacked FGM materials. Among existing methods Maxwell-Garnet equation [32] for calculation of effective for 2 layer dielectrics. As we need 3-layer effective calculation we need to derive the two equations for 3-layer dielectrics as follows:

3.3. Derivations for 3-Stage FGM with Materials A,B,C

When two layers or phases of dielectric materials are deposited on top of each other, calculation of their effective or resultant dielectric constant of this serially connected sheets of two dielectric materials, also called as, effective dielectric constant for A-B material (effective ) would be calculated by two models, first by Maxwell-Garnet approximation model [32], [41] as Eq.2;

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where are dielectric constants for material A and B and *f* is the volumetric filling factor for material A and (1 – *f* ) is the volumetric filling factor for material B in the two phase dielectric system of Fig 5.



**Figure 5.** Two phase dielectric system connected in series.

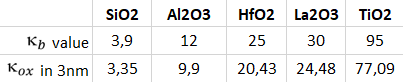
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To extend this theory for a three-phase system, we need to consider additional complexities due to the interaction between three different dielectric materials. If we denote the dielectric constants of the three materials as ​​, ​ ​, and ​ and their respective volumetric filling factors as *f*A​, *f*B​, and *f*C​ with *f*A​ + *f*B​ + *f*C​= 1, we need to derive an expression that considers all three materials. Thus we can;

* Calculate the effective dielectric constant ​​ for materials A and B using the Maxwell-Garnett equation.
* Consider ​ as one material and apply the Maxwell-Garnett equation again with ​ and ​ to find the overall effective dielectric constant , with *f*A​B​ + *f*C​= 1, finally as Eq.3,

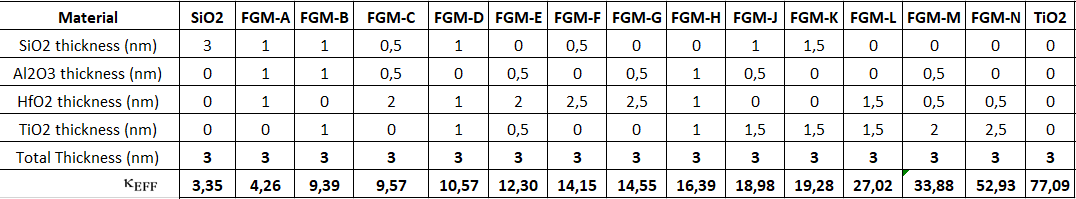
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**Table 4A.** Control Group: Thickness and bulk values and calculated (modified Penn model) dielectric constants values of 5 single material gate dielectrics for 3 nm thickness.



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**Table 4B.** FGM Group: Thickness and (applying modified Penn + MG model) values of 13 FGM gate oxide dielectrics between SiO2 and TiO2, shown as lower and upper limits of achievable within 3nm material thickness.



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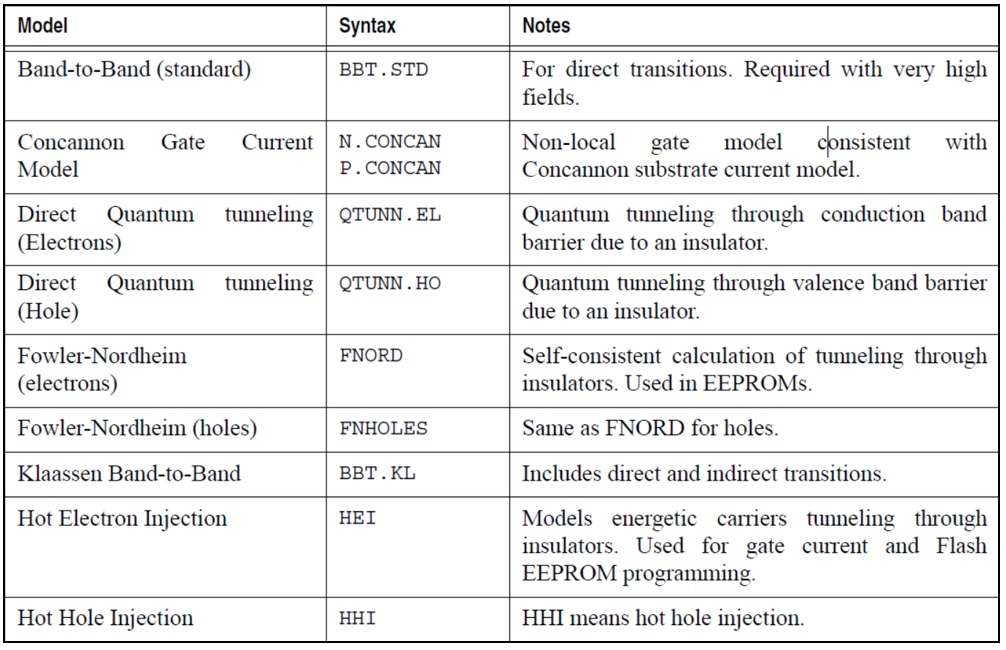
3.4. FinFET Modelling in Silvaco ATLAS Deckbuild Tool

We start with modeling our FinFET in Silvaco’s Atlas/Deckbuild. The family of such tools were used in many research to design and simulate the FinFET devices. The ATLAS Deckbuild simulation employing many standard recombination and continuity models like Shockley-Read-Hall, Schrödinger and Auger; used widespread for 2D/3D simulations of normal or heterogated single, double or triple-gated FinFETs [8],[31],[26].

3.5. Gate Leakage Current Modelling

In devices that have a metal-insulator-semiconductor (MIS) formation, the conductance of the insulating film would ideally be considered as zero. However, for the sub 0.5um generation of MOS devices there is considerable conductance being measured on the gate contacts [35]. In our case we used two lines of code for proper solvers to be activated in ATLAS/Deckbuild given in Appendix A, among tunneling-through-dielectric models available we used the hot electron/hole injection (HEI-HHI) tunneling model within ATLAS tool [35], so that gate-to-dielectric leakage current was properly and realistically modeled, which gave most accurate results comparable with [36].

**Table 5.** Summary of used models for tunneling and carrier injection for gate-dielectric leakage current in ATLAS [4.]



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3.6. Choice of Performance Metrics

Our performance metrics were selected as:

* **IG**, On-state gate leakage Current, in Amperes, leaks from gate metal through dielectric into the channel, when VGS = 0.75V in our case, needs to be minimized.
* **ION**, On-state Drain Current, in Amperes, when VDS = VDD (=1.2V in our case) and VGS= VDD , needs to be maximized.
* **IOFF**, Off-state Drain Current, in Amperes, when VDS = VDD and VGS = 0.0V, needs to be minimized.
* **ION/IOFF Ratio**, unitless, accepted and powerful measure of TFT design quality, needs to be maximized.
* **VTH**, Threshold Voltage, in Volts, the minimum VGS voltage that drain current ID slightly exceeds a limit current (1x10-7 A in our case) significant for the design, needs to be minimized.
* **SS**, Subthreshold Slope, in mV/decade, change in the gate voltage required to decrease the drain current ID by one decade, SS = ∆VGS/∆log(ID) , needs to be minimized.
* **DIBL**, Drain-Induced Barrier Lowering, in mV/V, represents the drain voltage VDS influence on the threshold voltage VTH, defined as DIBL = |∆VTH|/|∆VDS| , needs to be minimized.

as these are the primary parameters for evaluation of thin film transistors’ performance. [42]

3.7. Selection Process for the FGM – Creation of a Custom Figure of Merit

At the end of calculation process, we introduce and propose a unitless figure of merit as Equation-4:

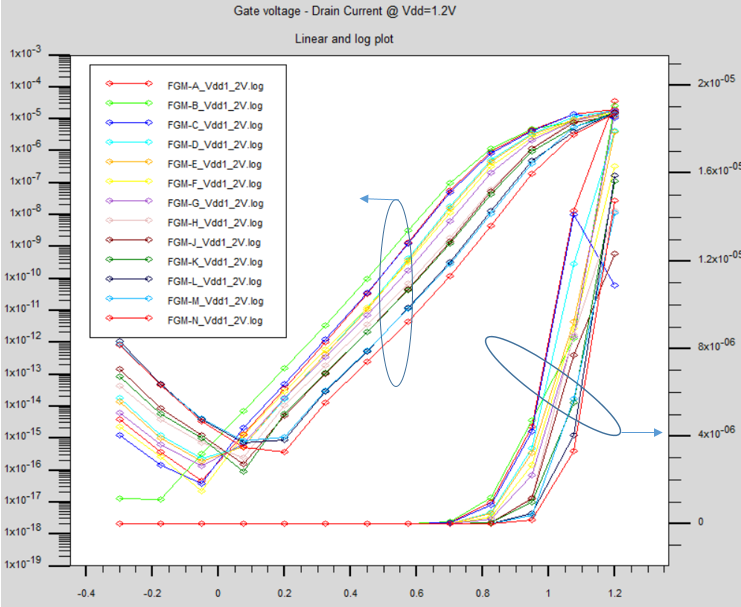
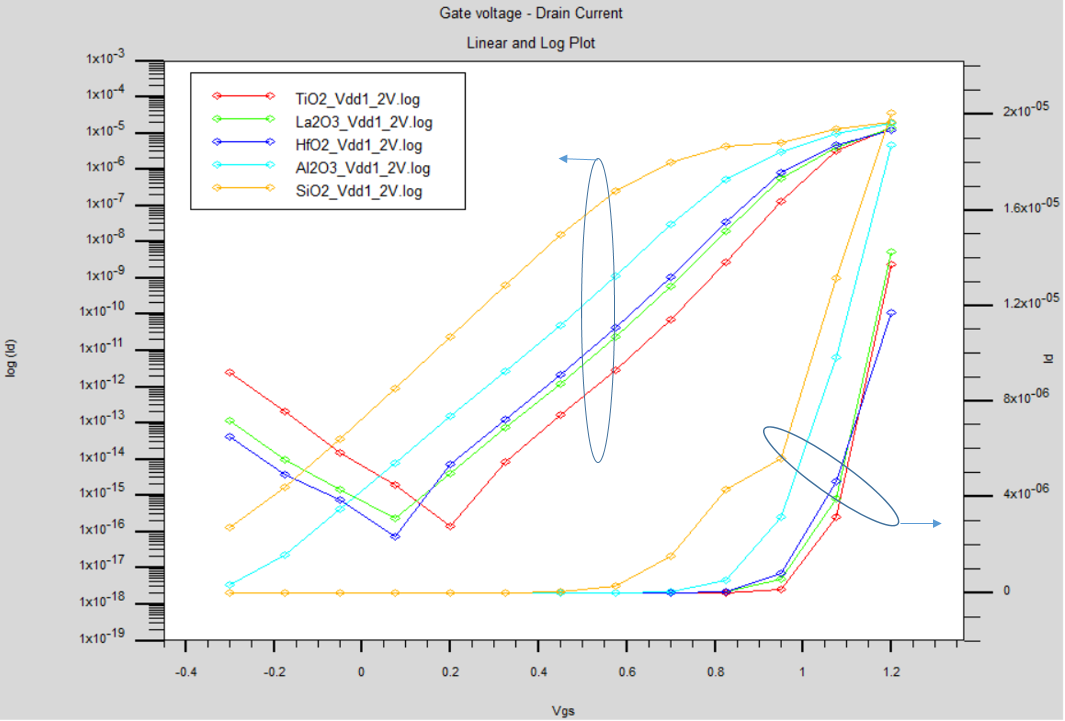
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with which we can evaluate the overall performance of FinFET under consideration. We developed this figure of merit that equally and mostly cares for IGL, ION/IOFF ratio and VTH, gives less importance to DIBL and even lesser importance to SS. Overall FOM value is multiplied by an arbitrary constant 97.62 to achieve best performing FinFET to appear with value equals to 100 and all other performance values to be normalized between 1 and 100. We compared the values of all single and FGM dielectric configurations so that it may help better to decide the selection among all configurations.

4. Results and Discussion

4.1. ID - VGS Transfer Characteristics

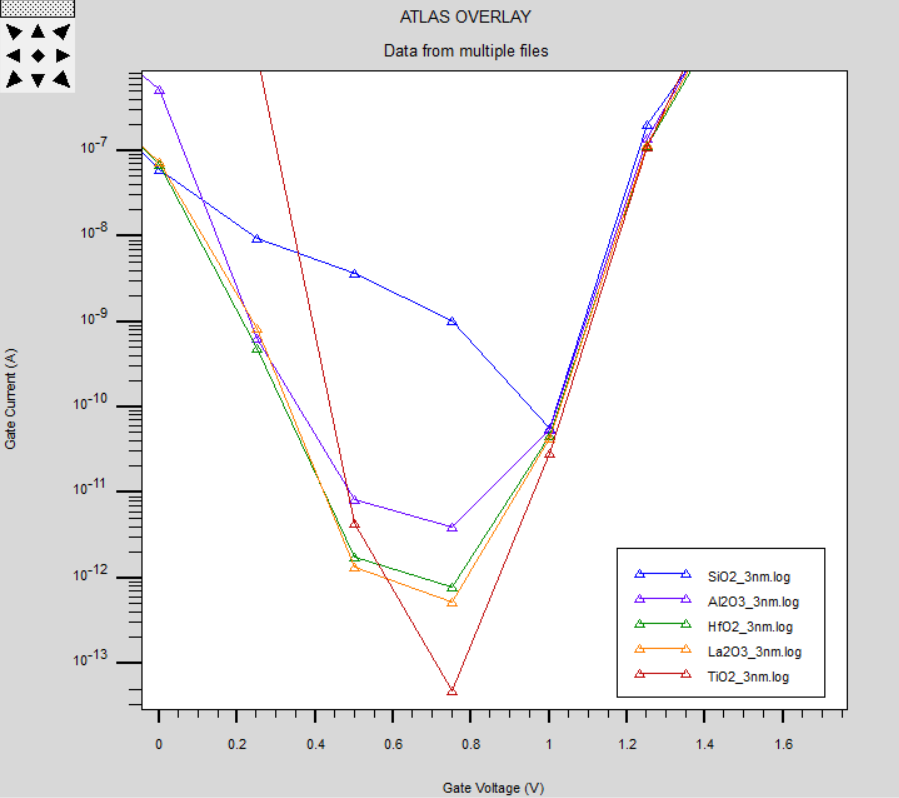
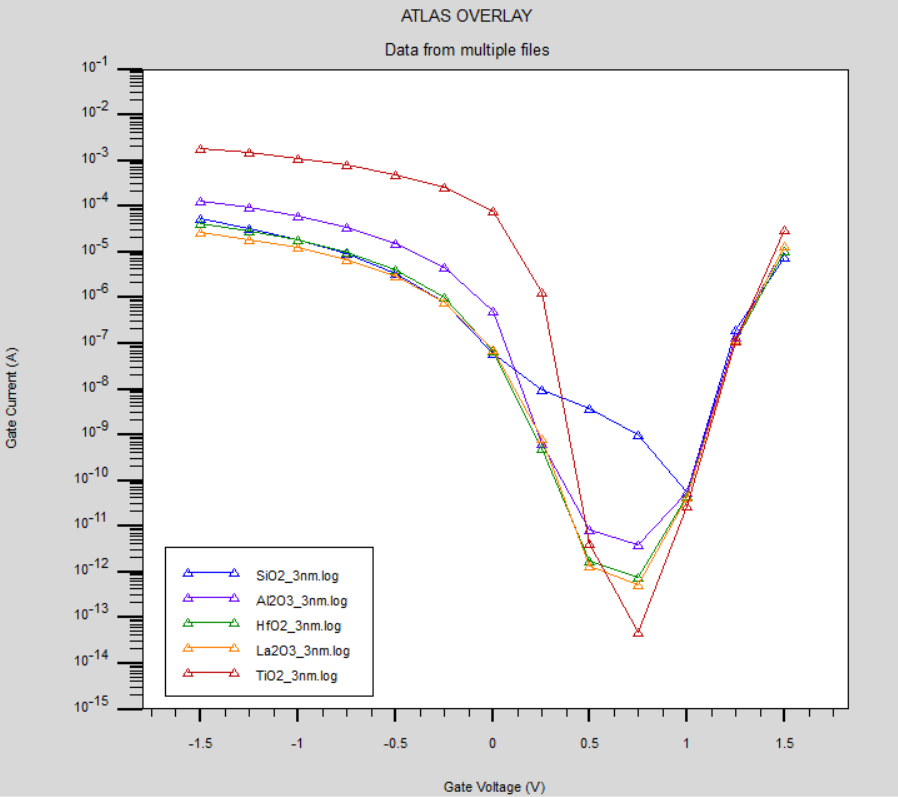
Figure 6. shows the drain current (Id) versus gate-source voltage (Vgs) characteristics for the FinFET device we examined with various gate dielectric materials. The threshold voltage is the point where the curve starts to steeply rise, which is a critical parameter for switching characteristics. The graph includes TiO2, La2O3, HfO2, Al2O3, and SiO2 as gate dielectrics. These materials are high-k dielectrics, with the exception of SiO2, which is a traditional dielectric material with a lower dielectric constant. TiO2 seems to have a higher on-current for the same gate voltage compared to the others, which may suggest better channel formation or a higher dielectric constant, which can modify the effective channel thickness. The choice of dielectric material significantly impact device performance. Higher-k materials like HfO2 and TiO2 may allow for thinner dielectrics, which can enhance gate control and reduce leakage currents, while also allowing for scaling down the device dimensions.



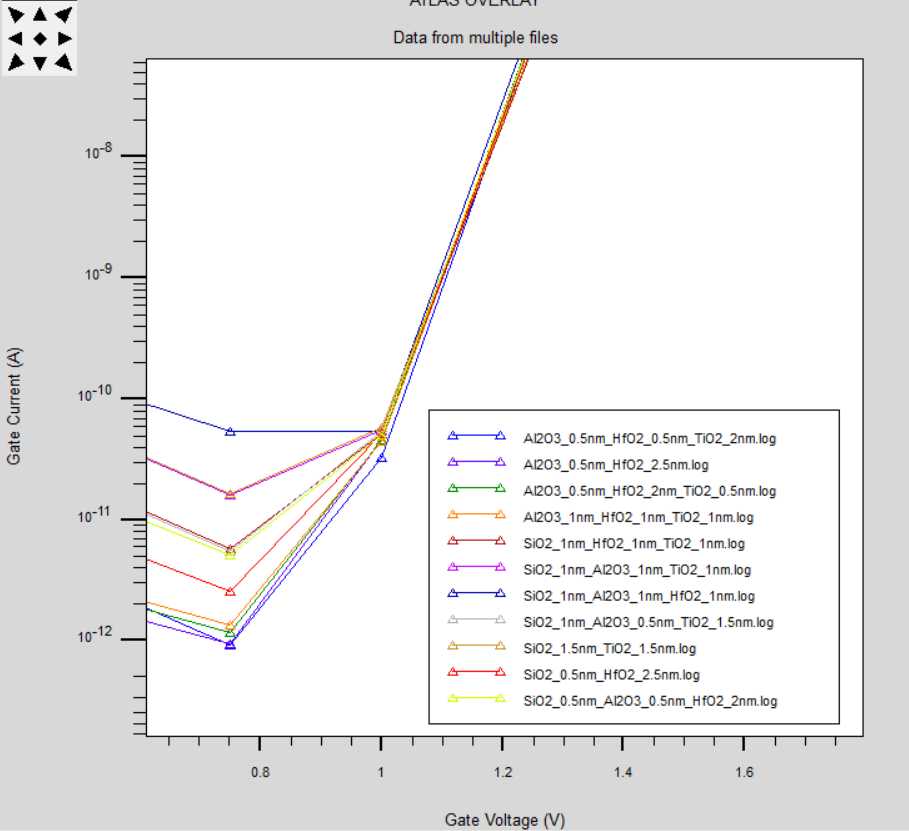
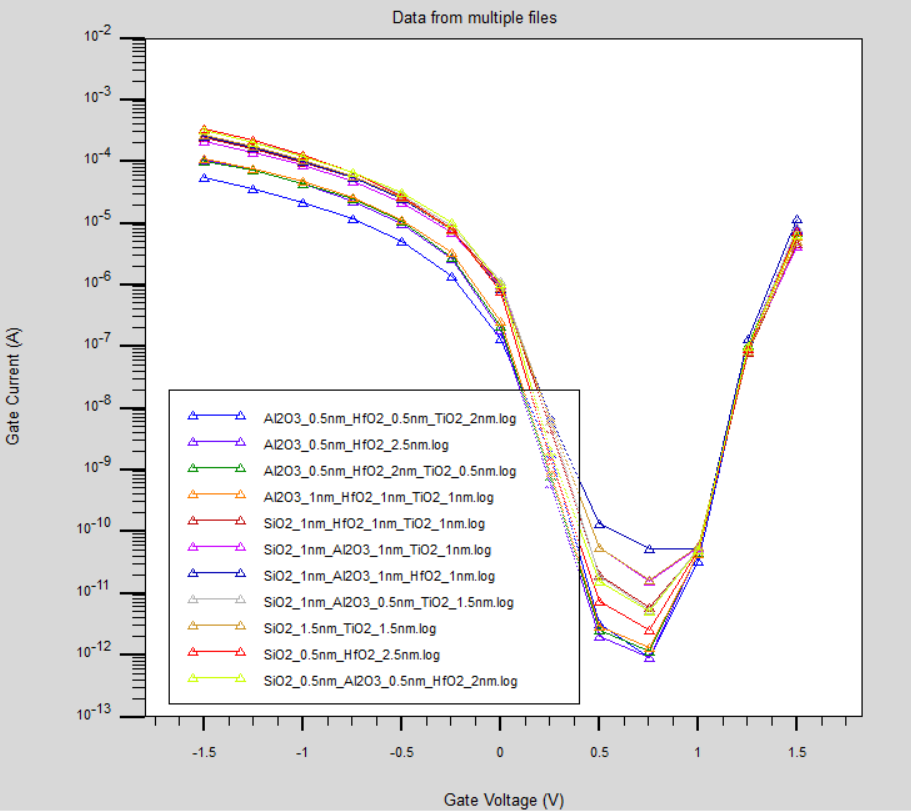
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**Figure 6.** a. ID for single material gate oxide dielectrics (control group) log(ID) –VGS (left) and ID –VGS (right) b. ID current for FGM-group of gate oxide dielectrics log(ID) –VGS (left) and ID –VGS (right).

4.2. IG per VGS Leakage Current



(a) (b)

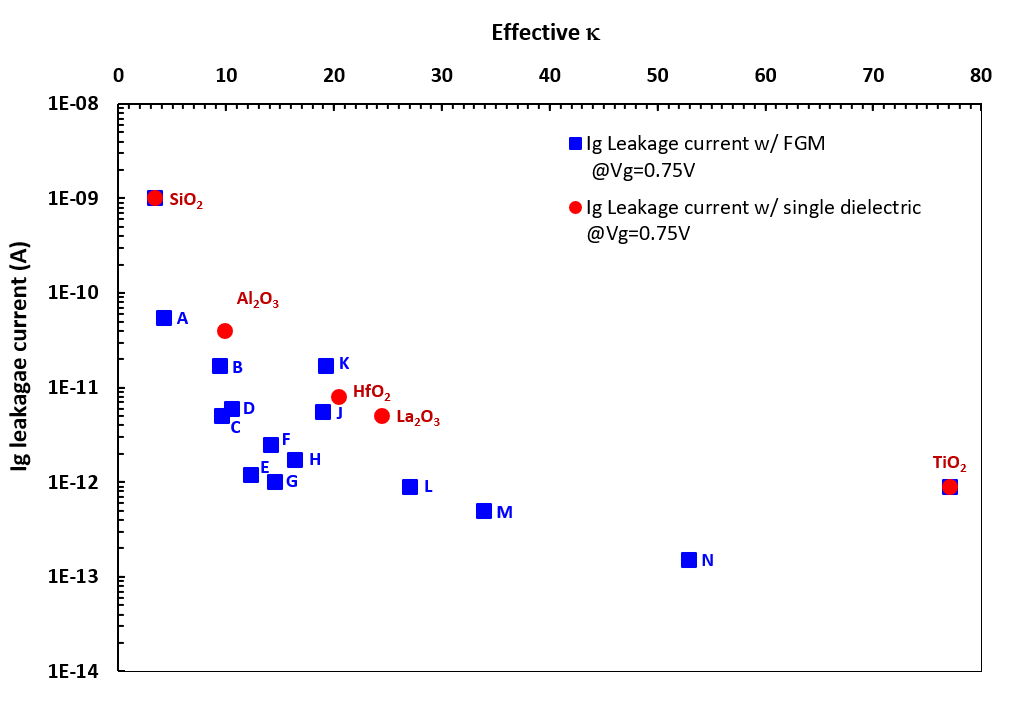


(c) (d)

**Figure 7.** a, 7b (zoom): IG leakage current for single material gate oxide dielectrics (control group) log (IG) –VGS 7c, 7d (zoom): IG leakage current for FGM group gate oxide dielectrics, log (IG) –VGS.

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[35]This graph shows the leakage current characteristics in the hot electron/hole injection model.[35] for traditional single-material gate dielectrics such as TiO2, with the lowest leakage current around 10-13 A at 0.75V for our specific FinFET under study, shown in Figure 1. The curves generally show a similar trend, with this leakage current decreasing with increasing gate-source voltage due to better depletion region formation. The right graph shows the leakage current for FinFETs with FGM gate oxides, labeled FGM-A through FGM-N. The curves are closely grouped and follow a similar trend to the control group, but with some variation between the different FGM materials. Lower leakage current is preferable, especially for memory devices such as EEPROMs where high IG can contribute to charge loss and memory degradation over time. The performance of FGMs in terms of IG appears to be similar to that of single-material dielectrics, suggesting that FGMs may provide a slight, non-significant advantage in reducing IG, but they do not exhibit any deficiency in device reliability.



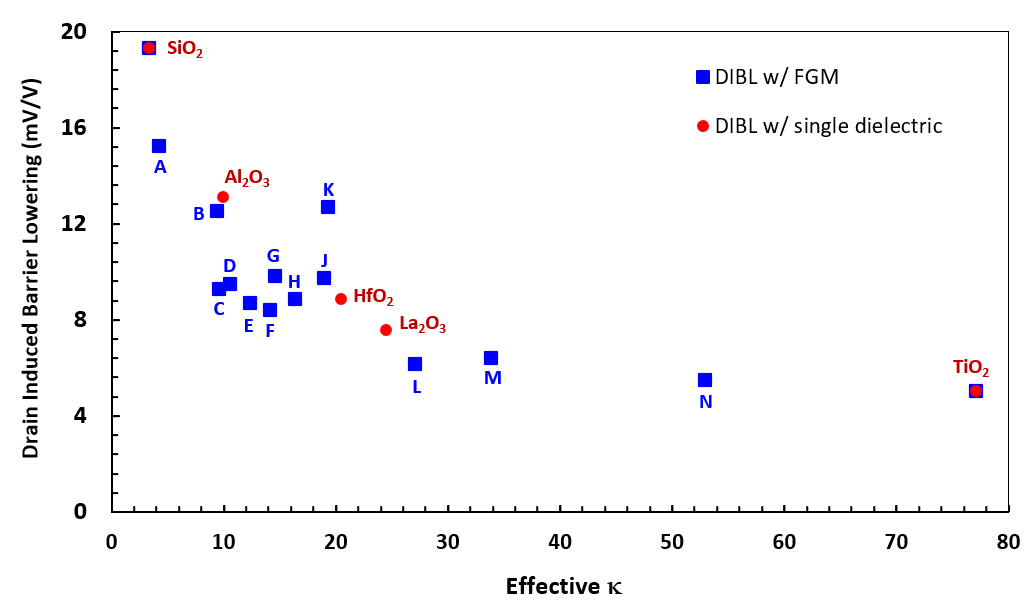
**Figure 8.** Ig Leakage Current for FinFET with single material and FGM gate oxide dielectrics (calculated with MG model).

We find that the use of FGM dielectrics has the potential to generate lower gate-to-channel leakage currents, and for FGM-N it is almost 53 times lower than that of the FinFET with single HfO2 dielectric, as it becomes apparent that interface effects are minimized when smoother dielectric constant transitions are fabricated from the channel to the gate material.

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4.3. Drain Induced Barrier Lowering

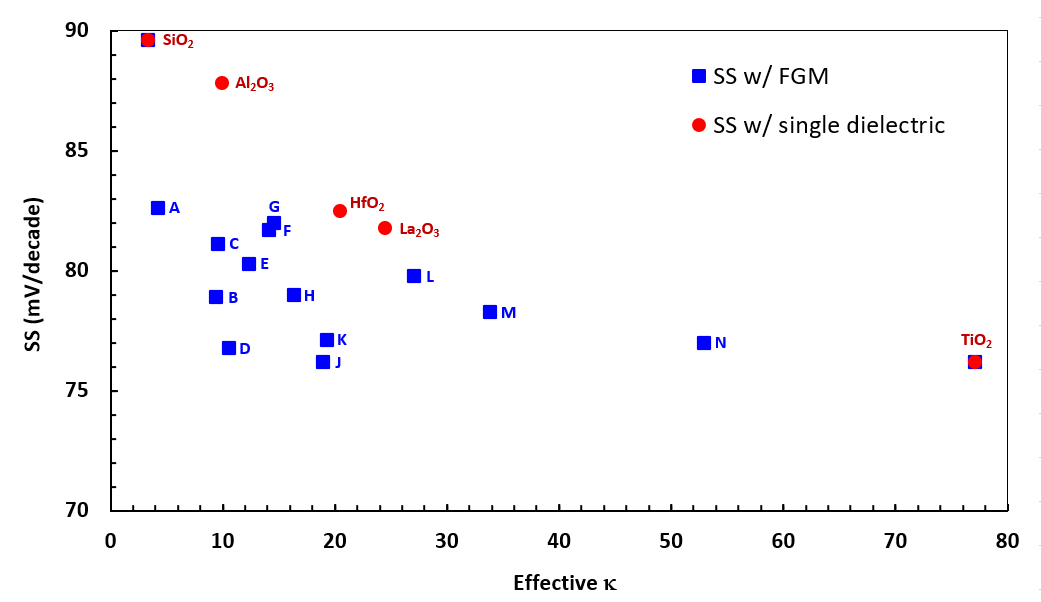
Figure 9 plots the Drain Induced Barrier Lowering (DIBL) against the effective dielectric constant (k) for different materials used in FinFETs. As DIBL is the short-channel effect where the drain voltage can influence the threshold voltage of the transistor, a lower DIBL value does generally better because it means the device has better control over the threshold voltage and is less susceptible to variations due to changes in the drain voltage. DIBL with single dielectric (Solid Line) represented the DIBL performance across a range of dielectrics for a standard single-layer dielectric material, starts high with SiO2 and then decreases significantly as the effective increases, showing improved performance for materials with higher κ values like HfO2, Al2O3, and TiO2. The trend suggests that as the effective dielectric constant increases, the DIBL effect decreases, which is a favorable outcome. DIBL values when using FGM techniques have peaks (labeled from A to N) that indicate where the DIBL is higher, possibly due to process variations, material properties or anomalies. DIBL performance of FGM’s seems best for FGM-N with 5.48 mV/V which is %38.2 lower than that of HfO2.



**Figure 9.** DIBL with single material and FGM gate oxide dielectrics

4.4. Subthrehold Slope

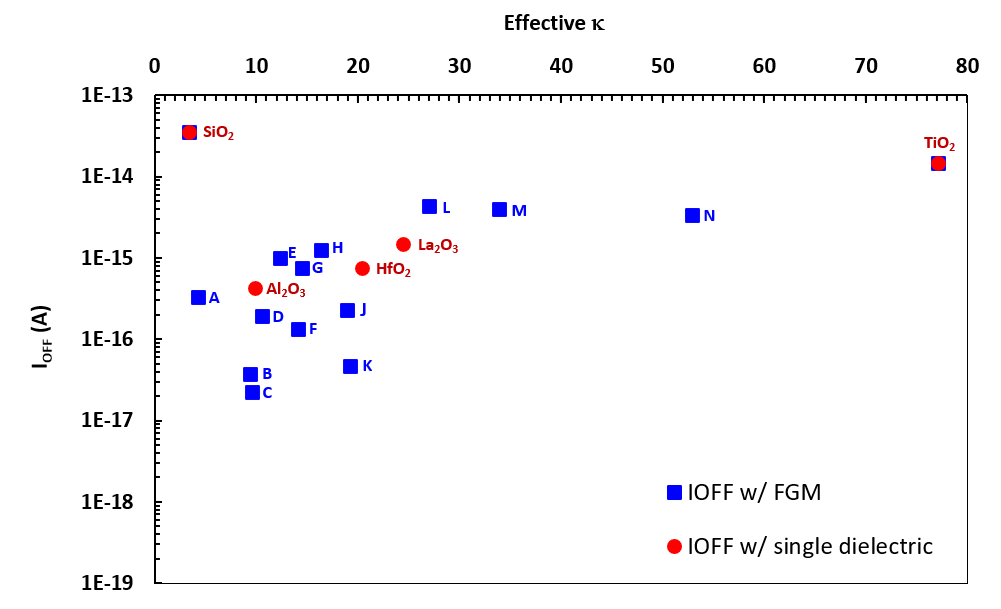
Subthreshold slope performance of FGM’s seems best for FGM-K with 76.2 mV/decade which is %7.64 lower than that of HfO2.



**Figure 10.** SS with single material and FGM gate oxide dielectrics A,B, C referansla tabloya

4.5. Off-State ID Current

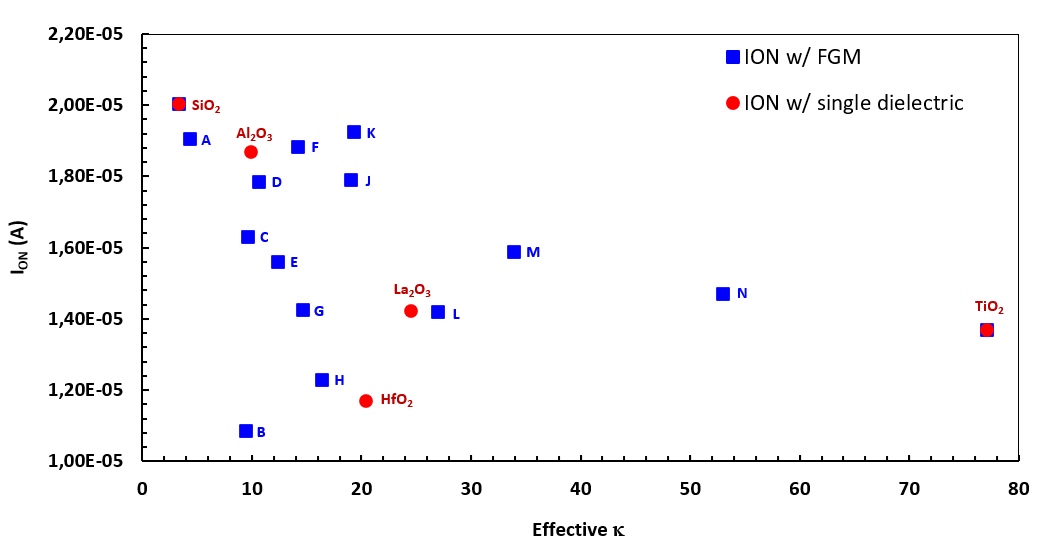
Off-State ID Current performance of FGM’s seems better for FGM-B with 2.23x10-17 A which is almost 2 orders of magnitude lower than that of HfO2.



**Figure 11.** IOFF with single material and FGM gate oxide dielectrics

4.6. On-State ID Current

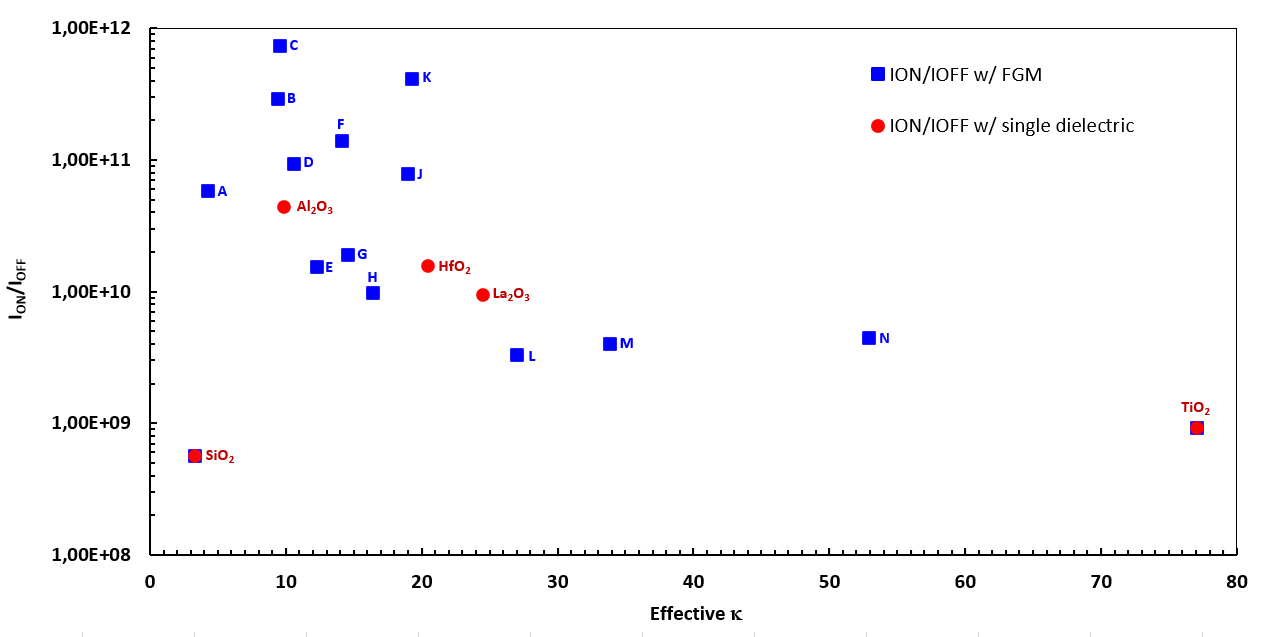
ON-State ID Current performance for FGM-K with 1.93x10-5 A which is almost %62 better than that of with HfO2.



**Figure 12.** ION with single material and FGM gate oxide dielectrics

4.7. ION / IOFF Ratio

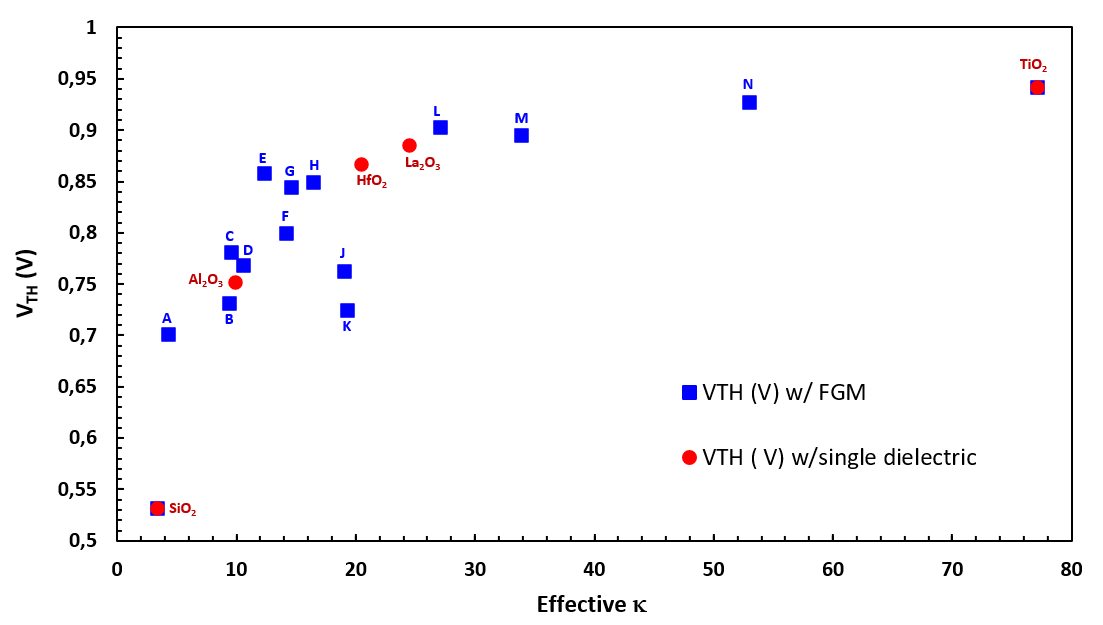
ION/IOFF ratio performance of FGM is better for FGM-C with 7.31x1011 which is almost 45 times better than that of HfO2.



**Figure 13.** ION/IOFF ratio with single material and FGM gate oxide dielectrics

4.8. Threshold Voltage VTH

VTH performance of FGM is better for FGM-A with 0.7012 V which is almost %19.2 better than that of HfO2.



**Figure 14.** VTH with single material and FGM gate oxide dielectrics.

5. Conclusion

The FGM technique may offer a way to engineer specific device characteristics, but it requires careful control and understanding of the material properties to achieve the desired outcomes consistently. Our results indicate that proposed FinFET with FGM gate dielectrics has lesser IGL up to 53 times, lesser DIBL up to %38.2, lesser SS up to %7.6, lower IOFF up to 2 decades, higher ION up to %62, higher ION/IOFF up to 45 times and lesser VTH up to %19.2.

**Table 6.**  values for each configuration of single dielectric and FGM configurations.

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|  |  |
| --- | --- |
| **Material** | **FOM\_FET** |
| **SiO2** | **9,5** |
| **Al2O3** | **20,6** |
| **HfO2** | **33,4** |
| **La2O3** | **43,0** |
| **TiO2** | **76,0** |
| **FGM-A** | **20,0** |
| **FGM-B** | **70,2** |
| **FGM-C** | **70,9** |
| **FGM-D** | **38,4** |
| **FGM-E** | **45,6** |
| **FGM-F** | **38,0** |
| **FGM-G** | **58,0** |
| **FGM-H** | **41,6** |
| **FGM-J** | **40,3** |
| **FGM-K** | **56,1** |
| **FGM-L** | **65,9** |
| **FGM-M** | **69,3** |
| **FGM-N** | **100,0** |

Looking at the values calculated by Equation-4, single dielectric gate oxides TiO2 has the best performance. HfO2 performance achieved 33.4 whereas FGMs B, C, K, L, M and N achieve better than HfO2 and entire single material dielectrics except TiO2.

FGM approach aimed to improve the gate's control over the channel and seemed to achieve a success with respect to the FOMFET selected as a figure of merit for overall FinFET performance, which can be always be customized due to importance of the performance parameter selected by the designer.

FGMs seem to provide some space to engineer new gate oxides between dielectric constants 35-95 and at least to try these as gate dielectric material. With respect to the same FinFET with single layer HfO2 gate dielectric performance, most FGMs showed superior performance. Within gate insulators and BOX structures, FGMs may provide versatile opportunities for optimizing FinFET devices.

5. Conclusion

We show k-graded gate oxides decrease adverse interface trap effects and decrease gate-channel leakage currents. A numerical analysis via introduction of a custom benchmark is conducted to show viability of usage of k-graded dielectric structures against conventional single layer high-κ dielectrics on 14-nm FinFET geometry. Impact on key electrical performance parameters are analyzed using SILVACO ATLAS TCAD as device simulation tool. Within 13 different 2- and 3-stage κ-graded stacked gate-oxide combinations some FinFET structures with κ-graded gate oxides (κG-FinFET) promise lesser gate leakage current up to 53 times, lesser drain induced barrier lowering (DIBL) up to %38.2, lesser subthreshold slope (SS) up to %7.6, lower drain off current (IOFF) up to 2 decades, higher drain on current (ION) up to %62, higher ION/IOFF up to 45 times and lesser threshold voltage (VTH) up to %19.2, with respect to the FinFET of same dimensions with a single layer HfO2 gate dielectric.

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